Process Development of Sidewall Spacer Features for Sub-300nm Dense Silicon FinFETs

Salwan Omar
MCEE
Microelectronics Engineering
Rochester, NY
salwanomar@gmail.com

Abstract*—An investigation of the ASML PAS5500 5X reduction i-line stepper and RIE systems capabilities of defining sub-300nm nitride sidewall spacers to create dense 200nm silicon FinFETs on a 400nm pitch has been experimentally undertaken in the SMFL at RIT. The work presented in this project involves photoresist over-exposure through annular illumination with NA equal to 0.6, sigma inner equal to 0.535, and sigma outer equal 0.9 to narrow down the critical dimensions of the photoresist features in the 200nm range. Diluted OiR620 photoresist with PGMEA 1:1 ratio is used to obtain a thin coating of 5.5nm film thickness. A thin aluminum layer was deposited and patterned and served as a hard mask for the subsequent oxide dry etching. Ideally, a thin conformal layer of nitride is deposited through low-pressure chemical vapor deposition (LPCVD) but more DOE is required to achieve smoother surface topology before silicon fin features can be adequately patterned.

I. INTORDUCTION

Photolithography techniques continue to enable the semiconductor manufacturing industry to meet their needs of achieving smaller, thinner, and faster device components for high performance applications. However, achieving smaller dense features requires new advanced patterning steps and techniques combined with chemical vapor deposition (CVD) and etch steps.

Methods for producing sub-lithographic feature sizes will be explored in this project. Mainly, photoresist overexposure and sidewall spacer lithography. Some lithography techniques are used after the photoresist exposure is processed through the stepper. The process is then carried on with physical, chemical, or tool modification techniques (i.e. Litho-Etch-Litho-Etch (LELE), mask biasing, double patterning, over-exposure, photoresist trimming, sidewall spacers, etc.) to achieve the desired pitch. The disadvantage of photoresist over-exposure and resist trimming is that the line and space ratio within the initial pitch is changed, one way of solving this problem is by altering the sidewall spacer line width by the conformal CVD film thickness.

One of the alternative avenues to achieve smaller and dense features is through the use of sidewall spacers. This approach is well-known in industry and uses LPCVD to deposit a thin conformal layer of nitride on top of the thermally grown oxide mandrel. It utilizes a reactive ion plasma etch to form the nitride sidewall spacers at the edges of the oxide mandrel. This process is considered to be done in-house at RIT's clean room to develop RIT's finFET manufacturing process to reduce the silicon fin width at a reasonable pitch.

In the past couple of years, RIT has been interested in improving the lithography process to print features below the ASML resolution limit so that they can take advantage of this device improvement and move forward to fabricate sub-300nm finFETs.

II. THEORY

A- patterning through Annular Illumination

i. Stepper system

The ASML PAS5500/200 5X reduction is an i-line stepper that has a variable 0.48-0.60 NA and both annular or conventional illumination. It has the capacity to image features down to 300-nm resolution through annular illumination with NA equal to 0.6, sigma inner equal to 0.535, and sigma outer equal 0.9. This stepper is is designed to handle and process 6" wafers and 6" reticles. The illumination source used in this system is a mercury light source with i-line filter.

ii. Equations

The resolution limit of any lithography stepper is defined by the Rayleigh criterion shown in equation 1. This equation specifies the minimum resolvable detail that can be imaged based on a given wavelength.

$$R = K1 * \frac{\lambda}{NA} \quad (1)$$

Salwan Omar is a student at Rochester Institute of Technology in the Department of Electrical and Microelectronic Engineering.
Email: salwanomar@gmail.com

K1 is a constant with a value of 0.5, λ is the wavelength of the light source, and NA is the numerical aperture of the lens. The K1 shown in equation 1 is a function of partial coherence:

$$K1 = \frac{1}{2(\sigma+1)} \quad (2)$$

σ is the ratio of the NA of the condenser lens to the NA of the objective lens. The sigma values of the ASML stepper are between 0.35-0.8. The depth of focus (DOF) of a system can be determined by the following equation:

$$DOF = \frac{\pm K2*\lambda}{NA^2} \quad (3)$$

Off-axis illumination is used in most illumination systems to illuminate the mask at an angle other than the normal angle to increase the depth of focus for the target CD and to allow more diffraction orders through the objective lens. The source shape is designed and optimized by the factor sigma for a specific mask to be imaged. The image performance is directly related to pitch size and directionality.

B- Photoresist Exposure

Photoresist is an organic, light-sensitive material which is applied to a flat substrate to form a thin film layer used to image features. In general, there are many different organic photoresists with different chemical properties that are used in photolithography. The uniqueness of organic photoresists is that the chemical properties will change when exposed to high-energy radiation, such as ultraviolet, deep ultraviolet (DUV), extreme ultraviolet (EUV), etc. After exposure to radiation, photoresist becomes either more or less acidic. Positive resist is photoresist which becomes more acidic after exposure to radiation because the exposed portion is cross-linked by UV radiation during the exposure and will become soluble in an alkaline solution optimized for the resist (e.g. for OiR620 resist the CD-26 developer is used) making it easier to remove. On the contrary, negative photoresist becomes less acidic after exposure to radiation and will remain on the substrate after development.

The total exposure energy applied is dependent on photoresist film thickness. Therefore, a thin layer of photoresist is necessary to achieve high resolution. The film thickness is a speed dependence function; a thinner film can be achieved by either diluting the photoresist or increasing the spin speed for a specific time and velocity.

A soft bake is always needed prior to exposure to drive out the solvents in the resist. Each photoresist requires a specific time and temperature; therefore, verifying the data sheet is always necessary before starting the process.

The hard bake step is obtained after developing the photoresist; this step is needed to harden the resist against etching process and to soften the patterned resist edges.

C-Thin Film deposition

i-Thermal Oxidation

Silicon dioxide (SiO_2) is a thin, uniformly-grown layer that is formed on a bare silicon surface in the presence of either water vapor or oxygen as an oxidant at an elevated temperature. There are two growth methods of oxidation known as wet oxidation and dry oxidation; both can be formed at a temperature range of 800-1400C. The following chemical equations are the reactions of thermal oxidation:

Wet oxidation: $Si + 2\ H_2O \rightarrow SiO_2 + 2\ H_2\ (g)$

Dry oxidation: $Si + O_2 \rightarrow SiO_2$

Wet and dry oxide always plays an important role in IC manufacturing acting as surface dielectrics, doping barriers, device isolation, etc. Ranges of the oxide thicknesses and their applications are shown in the table bellow.

SiO_2 Thickness (nm)	Application
10-50nm	Gate Oxide/Pad Oxide/LOCOS
200-500nm	Masking/Mandrel Oxide
>500nm	Field Oxide

Table 1. Oxidation Thickness Range and Application.

When a thick oxide film is required, wet oxidation is preferred over dry oxidation due to higher growth rates. However, wet oxidation has a lower density oxide and a lower dielectric strength. Also, faster oxidation tends to leave more dangling bonds at the interface, which can lead to current leakage. If the oxide layer is used as a hard mask, the quality of the film is not a major issue.

In this experiment, a layer of 400-nm wet oxide is patterned as a mandrel to form the nitride spacers on the edges.

ii. Sputtering

Sputtering is the concept of the momentum exchange between atoms and ions in the target material due to the collision, which is done inside a closed ambient under low pressure. This process is used to deposit a thin film layer of known material onto a smooth substrate by creating a gaseous plasma and accelerating the ions into the target material. The target is eroded by the ions and ejected as particles. The sputtered particles will travel in a straight path and arrive at the substrate, forming a thin layer of the material.

In a direct sputtering system, the substrate is positioned parallel to the sputtering target. As a general rule, the diameter

of the target should be at least 25% larger than the substrate to achieve uniform deposition. For example, a 16-cm diameter substrate would require a 20-cm diameter sputter target to be within 5% uniformity.

The sputtering yield is the rate of the sputtered atoms to the incident particles, which is shown in the following equation 4:

$$S = \frac{3\alpha 4M1M2E}{4\pi^2(M1+m2)^2Us} \quad (4)$$

α is related to the angle of the arriving ions, E is the energy of the incident atom, M1 is the mass of the sputtered atom, M2 is the mass of the incident atom, and Us is the atom's bonding energy.

The desired angle of the arriving ion measured from the normal to the surface is 60°. In some cases, the ion is most likely to backscatter if the angle of the arriving ion is less than 60°, forward scatter if the angle greater than 60°, implant to the surface when having a high energy, and stick to the surface when having a low energy.

Oxidation of the sputtered material can influence the sputter yield; pre-sputtering the target is always desired to remove the thin oxide layer.

iii. Thermal evaporation

Physical vapor deposition (PVD) techniques utilize evaporation of a material onto the surrounding substrates under vacuum using a high-temperature heating source. In this experiment, the CHA Flash Evaporator was used to evaporate pure aluminum onto the substrates. The evaporation of the aluminum was done with a wire feed on a highly heated plate. Once the wire touches the heated plate, aluminum atoms vaporize and make their way to the surrounding substrates. The pressure inside the Flash Evaporator chamber determines the mean free path length (MFPL), which is how far can the aluminum atom travel before it collides with an oxygen particle. The evaporated aluminum thickness and uniformity directly depend on the setup of the substrate holder; the further the substrates are from the target, the greater the chance for aluminum atoms to collide with oxygen molecules which will result in less aluminum atoms reaching the substrate surface. This produces a thinner film layer with higher sheet resistance. Substrates closer to the evaporation source are usually processed by placing the substrate holder at an angle. As the distance between the source and the substrate decreases, it will result in a thicker, non-uniform film with low sheet resistance. The CHA Flash Evaporator has a rotary mechanism installed to rotate the substrates while depositing the material to achieve a uniform film deposition; it also has a programmable thickness monitor to either manually or automatically terminate the evaporation by closing the shutter when it deposits the desired thickness.

iv. Low-Pressure Chemical Vapor Deposition (LPCVD)

The LPCVD system used in this experiment is a hot wall system. This system uses heat to initiate a chemical reaction on the surface of the substrate. This technology is commonly used to conformally deposit silicon nitride, polysilicon, and silicon dioxide with a low pressure of ~100mT and a temperature range of 300C to 800C. The low pressure is used to suppress the unwanted gas reaction and improve the deposited film uniformity across the wafer.

The operation of the tube starts with the evacuation to a low-pressure range between 1 mTorr to 1 Torr. Once the tube reaches the desired low pressure, it is then heated to the process temperature of the deposited film which corresponds to the decomposition temperature of the precursor gas. The selected gas is injected into the process tube where it diffuses uniformly and reacts with the surface of the wafer, creating the solid phase of the desired material. The excess gases are then pumped out of the system through the burn box.

Silicon nitride thin films can be deposited via two different chemical reactions: a reaction between ammonia (NH_3) and silane (SiH_4) or a reaction between ammonia and dichlorosilane ($SiCl_2H_2$). The following chemical equation is for the silane reaction which occurs at 800C:

$$3SiH_4 + 4NH_3 \rightarrow Si3N_4 + 12H_2$$

The dichlorosilane reaction occurs in LPCVD between 700C and 800C and is described in following reaction:

$$3SiCl_2 + 4NH_3 \rightarrow SiN_4 + N_3 + 6HCl + 6H_2$$

The advantage of using LPCVD systems for thin film deposition is that the deposited film is more uniform and has fewer defects. However, the higher temperature can set limitations on the type of the substrate and the gaseous materials prior to the deposition.

D- Reactive Ion Etch (see page 44)

i. Dry etching 38

The technology of reactive ion etch (RIE) processing is a dry etching technique widely used in the manufacturing industry. It employs the concept of a chemically reactive plasma under the prescence both an electrical field and low pressure to remove the desired materials from the substrate. A typical RIE process consists of a high-frequency RF power source connected to two parallel electrodes inside a cylindrical vacuum chamber. The wafer is placed on the grounded plate (cathode) to be isolated from the other parts of the chamber. Reactive gases enter the chamber from one end and exit through a vacuum system usually connected to the bottom of the chamber. The pressure is usually in the range of 1 mTorr – hundreds of mTorr to sustain the plasma; gas flow rates can be tuned to achieve a low pressure level. Gas selection is a process dependent factor; fluorine is the main etchant component in a SiO_2 etch, CHF_3 creates and sustains a plasma

and additionally creates fluorine radicals to combine with silicon and desorb SiF_4. Hydrogen is combined with fluorine to further reduce the silicon etch. Addition of O_2 results in organic/carbon removal; the O_2 flow must be well-controlled to minimize the etch rate of the organic materials, especially if the organic materials are utilized as a mask for subsequent etching processes. Fluorocarbon gas will form the C-F polymer which is deposited on the side walls of the vertical features to reduce the isotropic etch rate. Argon gas is often introduced into the chamber to act as a physical sputtering gas to remove the polymer build-up on the horizontal surfaces. The addition of N_2 might be required to improve heat transformation.

The aim of this project is to have a high degree of anisotropy; the following equation can be used to determine the degree of anisotropy:

$$A = \frac{z - x}{z} \tag{5}$$

x and z are is the horizontal and vertical direction, respectively. Generating a highly-vertical etch rate and minimal horizontal etch rate requires higher power, lower pressure, and an increase in polymer formation on the vertical side walls.

Various types of plasma parameters can affect the RIE such as pressure level, input power, and the selected gas flow rate. These parameters must be well-controlled to implement and characterize the desired etching process.

III. EXPERIMENTAL PROCEDURE

i. Mask Design

The first step in this project was to design a simple mask that had an array of vertical and horizontal lines with different critical dimensions and pitch size. This design features a variety of pitch sizes and duty ratios to demonstrate the possible dimensions when fabricating the device. The mask design was drawn in Mentor Graphics and fabricated in the Heidelberg.

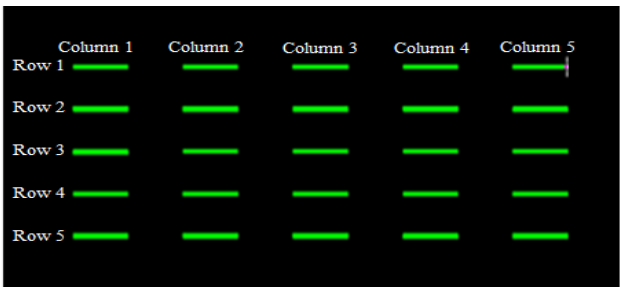

Figure 1. Mask Array.

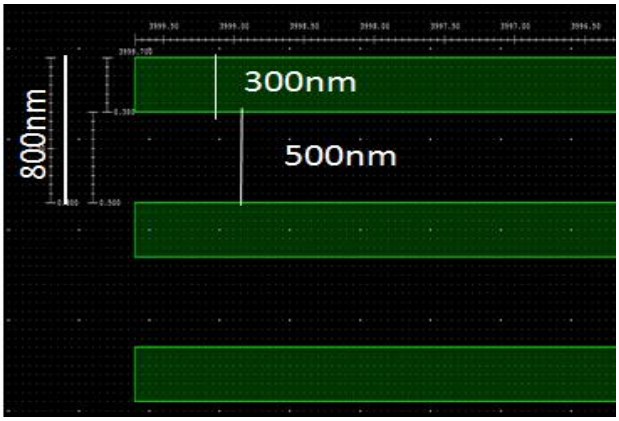

Figure2. Critical Dimensions of Selected Location (Column1, Row1).

		Column 1	Column 2	Column 3	Column 4	Column 5
Row1	L (nm)	300	300	300	300	300
	S (nm)	500	450	400	350	300
	P (nm)	800	750	700	650	600
Row2	L (nm)	350	350	350	350	350
	S (nm)	500	450	400	350	300
	P(nm)	850	800	750	700	650
Row3	L (nm)	400	400	400	400	400
	S (nm)	500	450	400	350	300
	P (nm)	900	850	800	750	700
Row4	L (nm)	450	450	450	450	450
	S (nm)	500	450	400	350	300
	P (nm)	950	900	850	800	750
Row5	L (nm)	500	500	500	500	500
	S (nm)	500	450	400	350	300
	P (nm)	1000	950	900	850	800

Table 2. Array Size and Critical Dimensions of the Horizontal Lines.

ii. Proposed Process procedure

The proposed experimental procedure to achieve sub-300nm silicon fins are shown as follows:

(1) RCA clean all of the process wafers prior to the silicon dioxide growth

(2) A layer of 400nm wet SiO2 is thermally grown.

(3)100nm of aluminum is evaporated on top of the SiO2 serving as a hard mask.

(4) 150nm of I-CON 7 ARC is coated on the aluminum followed by coating 560nm of diluted 1:1 OiR620 photoresist.

(5) Desired features (400L × 500S) are over-exposed.

(6) RIE I-CON 7 ARC layer in the Drytek.

(7) RIE the Aluminum layer in the LAM4600; use SpectraSuite software to detect the intensity profile for etch stop to insure a complete aluminum etch.

(8) RIE the SiO2 layer in the P-5000 chamber C (wafer back must be cleared of oxide to prevent arcing).

(9) Aluminum strip prior to LPCVD.

(10) Deposit a 200nm conformal layer of nitride through LPCVD.

(11) RIE the nitride layer in the DryTek to form the sidewall spacers on the edges of the oxide mandrel.

(12) strip the oxide mandrel in 10:1 BOE.

(13) RIE silicon in the Drytek.

(14) strip the nitride sidewall spacers in hot phos.

SEM images are required after each etching step (including resist exposure) to confirm the desired results.

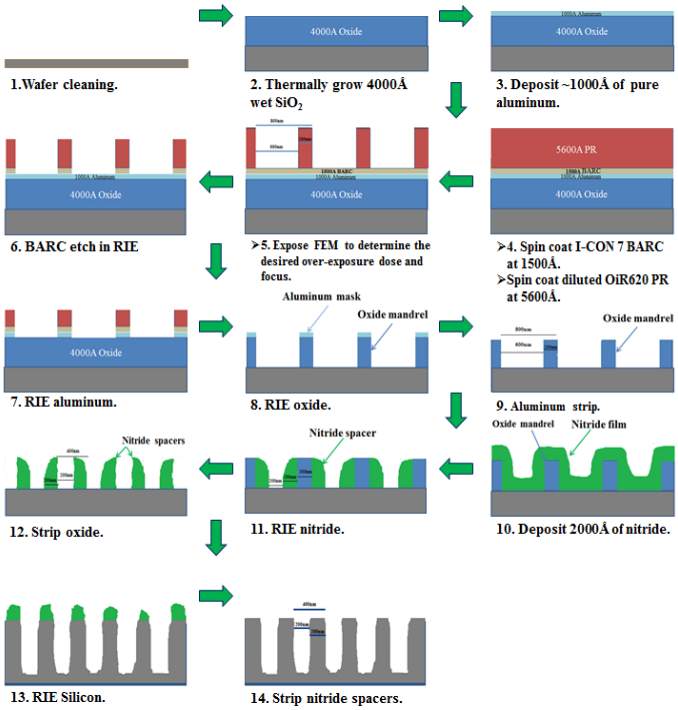

Figure 3. Proposed Process Flow.

IV. RESULTS AND DISSCUTIONS

The swing curve simulation for the film stack is crucial in the determination of the optimum I-CON 7 ARC thickness which results in the highest contrast. The simulation was performed in PROLITH to demonstrate the substrate reflectivity and the benefit of optimizing the I-CON thickness. Figure 4 shows the substrate reflectivity of the Oir620 photoresist on BARC on oxide. The BARC is necessary to have on top of the oxide film to minimize substrate reflectivity, eliminate standing waves in the photoresist, and provide ultimate critical dimensions. It is desired to have the substrate reflectivity to be less than 10 percent, thus, the I-CON 7 thickness was found to be optimal at 100 nm for this procedure. However, the aluminum layer was also considered in this investigation to serve as a hard mask. Figure 5 shows the substrate reflectivity of the Oir620 photoresist on BARC on aluminum. The I-CON ARC thickness was found to be optimal at 150 nm for this procedure.

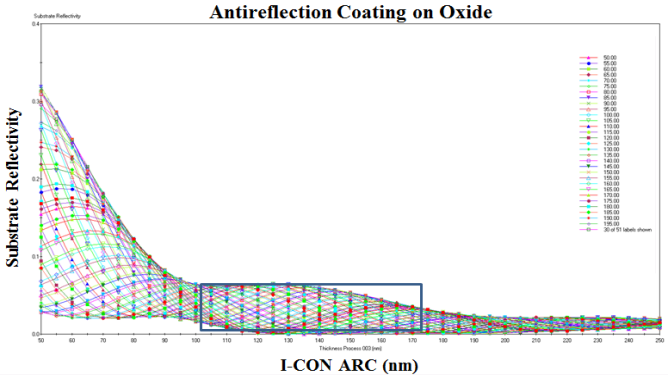

Figure 4. Substrate Reflectivity When Varying I-CON 7 Thickness and Oxide Thickness.

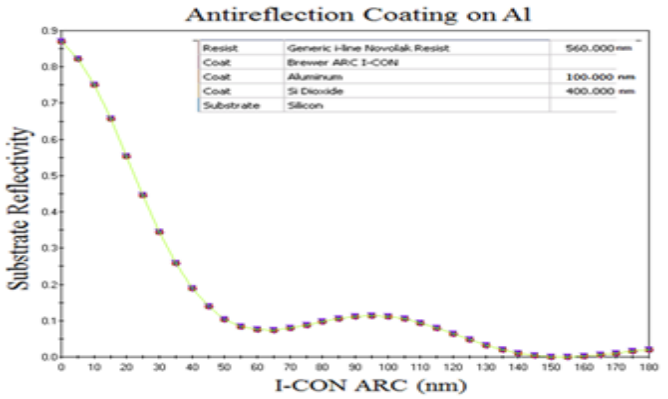

Figure 5. Substrate Reflectivity when Varying I-CON 7 Thickness on Aluminum.

The first fabrication step was to RCA clean all of the process wafers and thermally grow a thin layer of wet SiO_2. The RCA procedure is depicted in figure 6. This is the standard wafer cleaning procedure at RIT and it is normally performed prior to a high-temperature oxidation process.

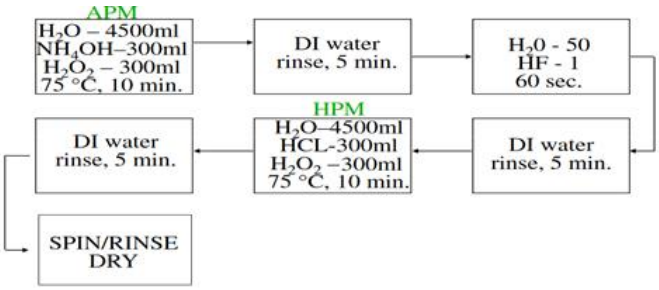

Figure 6. RIT's Standard RCA Cleaning Process.

Water, hydrogen peroxide, and the ammonium hydroxide mixture removes organics from the surface of the wafer such as photoresist and fingerprints. Hydrogen peroxide breaks down into H_2O and O_2; O_2 protects from being etched in ammonium hydroxide. Hydrofluoric acid removes oxides formed previously from the ammonium hydroxide as well as any native oxide. Water, hydrogen peroxide, and the hydrochloric acid mixture removes any inorganic residues and heavy metals.

Oxidation of the substrate surface is performed right after the RCA clean. A thin, 200-nm layer of oxide is thermally grown on the first set of wafers using the Bruce Furnace Tube 1 and recipe *193 Cabrera 2000 wet ox*. Oxide thickness measurements are summarized in table 3:

Wafer ID	Mean (nm)	Std.dev.	Min (nm)	Max (nm)	Range (nm)
Aa	182	2.30%	175	192	17
Ab	186	2.50%	177	198	21
Ac	188	3.50%	177	206	29
Ad	189	3.30%	178	207	28

Table 3. First Set of Thermal Oxide Measurements.

The BARC used in this experiment is Brewer Science ARC i-CON 7. The Oir 620 photoresist is diluted with PEMEA with 1:1 ratio. The Oir620 resist spin curve is generated by coating several silicon dummy wafers to determine the optimal resist thickness.

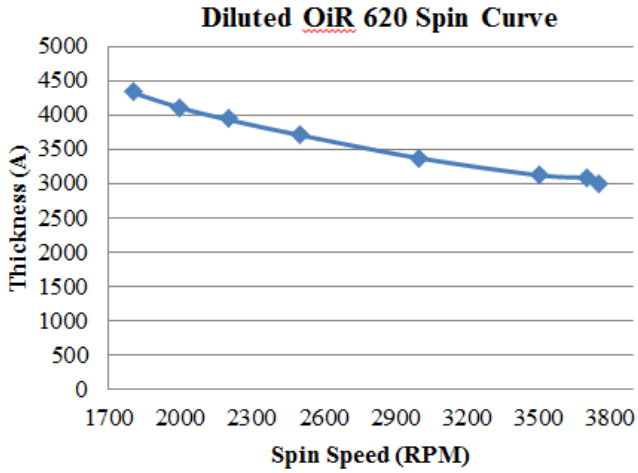

Figure 7. OiR 620 Spin Curve.

The oxide layer is then coated with BARC and photoresist at the determined optimal thicknesses.

A focus-exposure-matrix (FEM) is a critical tool to verify and evaluate the lithographic process performance of the optical system, chemistry, and critical dimension. FEM is used in this experiment to analyze the process latitude of the ASML stepper. The ASML stepper has a variable NA, conventional illumination, and annular illumination capability which allows the imaging of sub-300nm features. The numerical aperture value is set to 0.6, the sigma inner and outer are set to 0.535 and 0.9, respectively, the dose range is set at 150mj ±10mj and the focus range is set at -0.5um ± 0.1.
Figure 8 shows the FEM that was performed using the ASML stepper and the designed mask to determine the desired CD and pitch size.

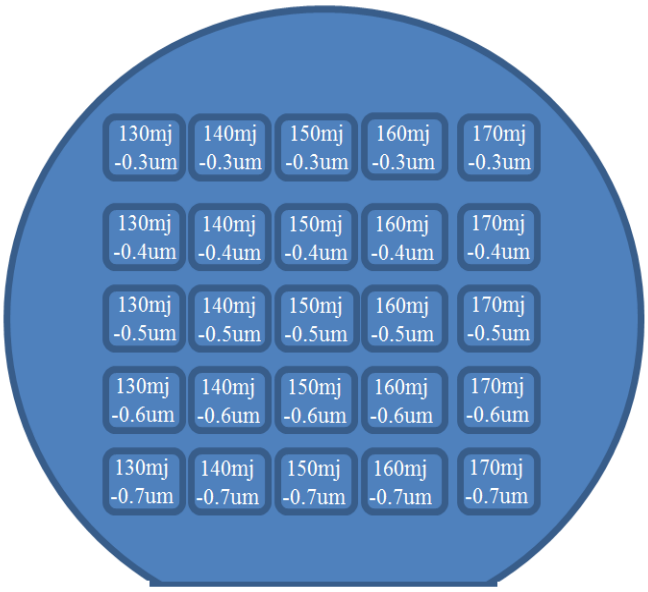

Figure 8. Focus Exposure Matrix.

The best dose and focus was found to be optimal at 170mj and -0.4, where it over-exposed; the desired 400 × 500nm mask features were found to be 280 × 570nm L/S. Figure 9 shows an SEM image of the over-exposed feature on oxide layer:

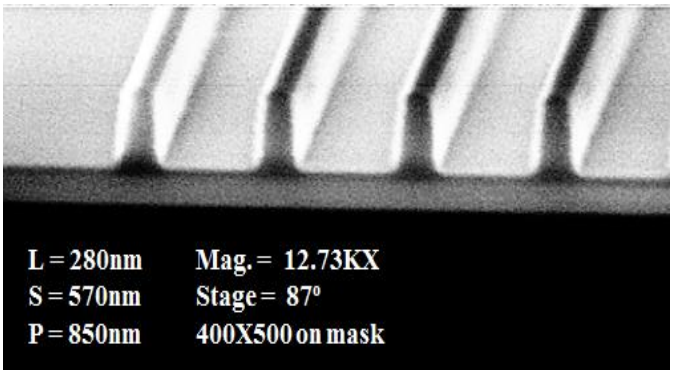

Figure 9. Over-exposed 400X500nm Features.

This condition was applied to the process wafer and followed by an RIE of the BARC to clear the space in-between the resist lines allowing the subsequent oxide etching to define the oxide mandrels. Both the I-CON ARC and oxide etch processes were performed on dummy non-patterned wafers by utilizing the DryTech RIE to determine the etch time. Dummy wafers went through the soft bake, development, and hard bake processes to mimic the fabrication process as accurately as possible when measuring and determining the etch rates.
Figure 10 shows the I-CON 7 and Oir620 etch rate using a known recipe.

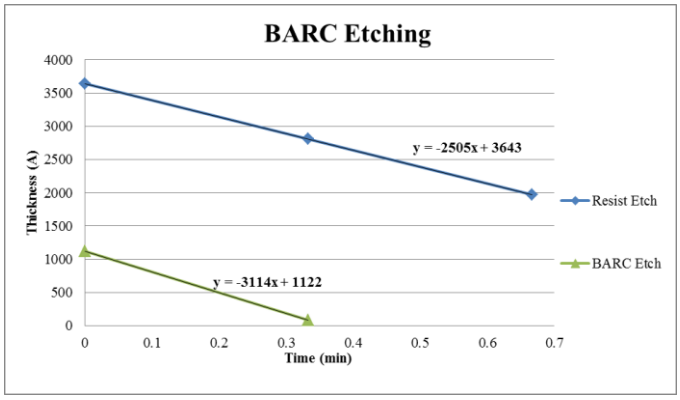

Figure 10. I-CON 7 and Oir620 Etch Rates in the Drytek RIE.

Due to the sensitivity of I-CON 7 and OiR620 to O_2 (given they are both carbon-based polymers), 30 to 40 nm of the photoresist was lost prior to the BARC plasma etching. However, the difference in film thickness provided the benefit to be on the safe side when etching I-CON 7. The etch rates of the I-CON 7 and Oir620 were found to be 311 nm/min and 251 nm/min, respectively.
Figure 11 shows the measured thermal oxide and OiR620 etch rates using a known recipe.

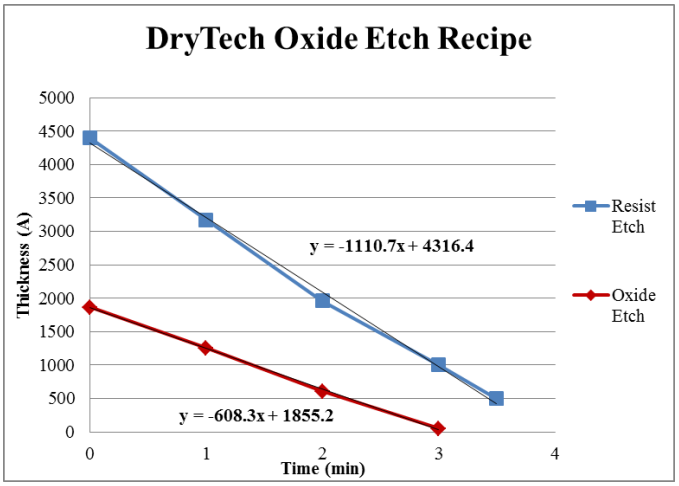

Figure 11. Oxide and Oir 620 Etch Rates in the Drytek RIE.

The oxide etch rate and the OiR620 etch rate were found to be 61 nm/min and 111 nm/min, respectively. Since the resist etch rate to the oxide etch rate is 2:1 and the resist thickness at this step was about 400 nm, the etch time needs to be well-controlled to not over-etch the reminding resist causing the oxide lines to disappear.

At this stage, the process wafers were ready to be processed using the above information including exposure and etch rates to create the oxide mandrel for the subsequence CVD nitride and RIE nitride to define the nitride spacers.

Figure 12 shows the pattern transfer of the photoresist to the oxide after the I-CON ARC 7 is ashed from the spaces.

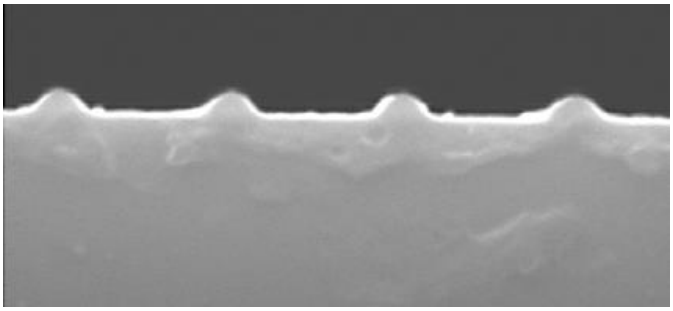

Figure 12. Oxide Lines on Silicon Substrate.

The pattern transfer of the photoresist did not show a vertical sidewall profile on the oxide mandrel. This effect is due to the etch rate of photoresist to oxide is approximately 2:1 and the fact that the photoresist etches in the lateral direction, making the resist to be a soft make to protect the oxide.

To overcome this problem, an aluminum hard mask was utilized as well as doubling the oxide thickness to 400 nm to have a better observation of the oxide mandrel sidewall profile. A sputtering technique was used to sputter 100 nm aluminum on top of the 400 nm thermal oxide layer, followed by a lithography and an RIE step to define the desired features on aluminum.

Table 4 represents the oxide measurements after the wet oxidation process. A 400-nm layer of thermal oxide was grown on the second set of wafers that has four new wafers (A1-A4) and four reworked wafers (A5-A8).

Wafer ID	Mean (nm)	Std.dev.	Min (nm)	Max (nm)	Range (nm)
A1	398	(0.58%)	39.4	40.4	10
A2	399	(0.57%)	39.5	40.4	9
A3	396	(0.52%)	39.3	40.1	8
A4	398	(0.54%)	39.4	40.2	8
A5	376	(0.67%)	37.2	38.2	9
A6	376	(0.72%)	37.1	38.2	10
A7	375	(0.76%)	37.1	38.1	10
A8	379	(1.1%)	37.2	38.2	15

Table 4. Second Set of Thermal Oxide Measurements.

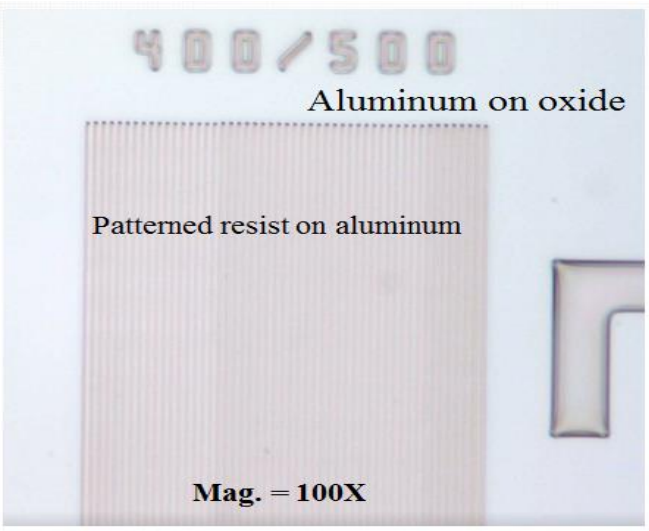

Figure 13. OM Image of Photoresist Pattern on the Sputterd Aluminum Layer.

Etching aluminum required a plasma intensity endpoint detector to monitor the plasma intensity profile as it etches through aluminum layer.
The SpectraSuite software tool was used to detect the intensity profile of the RIE process.

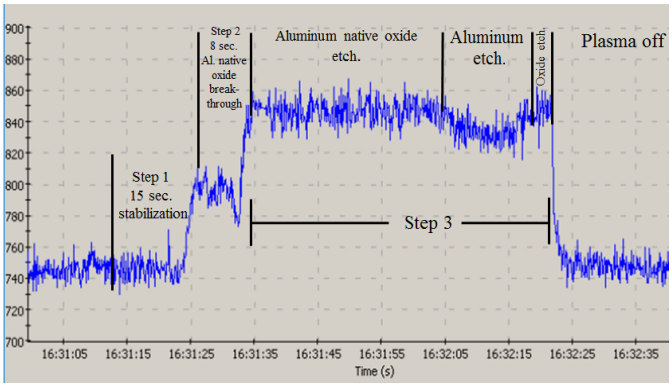

Figure 14. Aluminum Endpoint detection.

Step 1 is a 15-second stabilization step to flow the appropriate gases, step 2 is the initial breakthrough etch of the aluminum oxide Al_2O_3 (native oxide) layer, step 3 is where the aluminum etch will occur after the etching chemistries break through the native oxide layer. As seen in the figure 14, the plasma intensity decreases as it etches the aluminum layer in step 3 and then increases again when it starts to etch the thermal oxide layer; once this happens, the endpoint is observed and the run is manually terminated. It is important to keep the aluminum thickness thick enough to be detected by the intensity detector; however, the limitation on the resist thickness should also be considered as the resist would completely etch off before the aluminum layer and cause the desired features of aluminum to be over-etched.

Figures 15 and 16 show the RIE result for the sputtered aluminum.

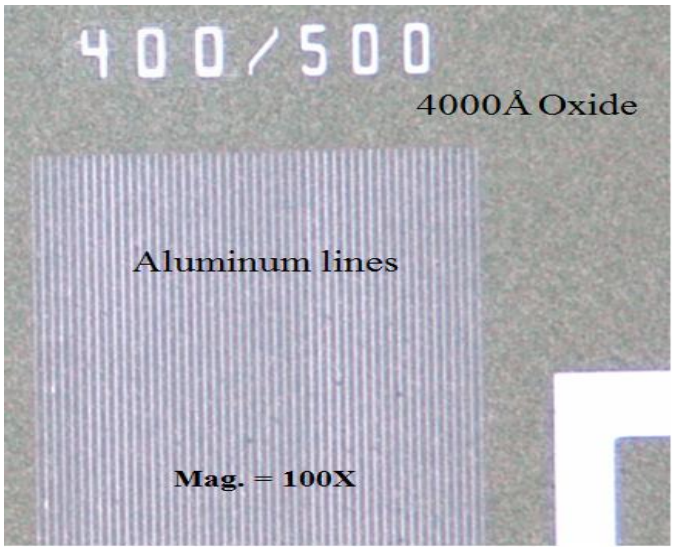

Figure 15. OM Image of the Aluminum Hard Mask on Top of the thermal oxide layer.

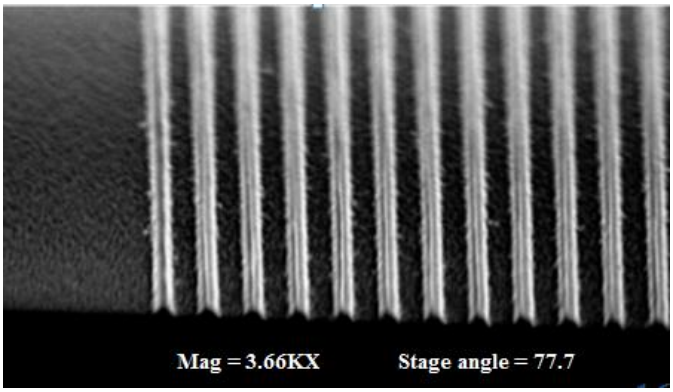

Figure 16. SEM Image of the Aluminum Hard Mask on Top of the Thermal Oxide Layer.

The photoresist pattern successfully transferred to the sputtered aluminum layer creating aluminum lines and spaces with dimensions of 221nm and 612nm, respectively.

Figure 17 shows the etch rate of the oxide done on a un-patterned oxide wafer utilizing a different RIE tool.

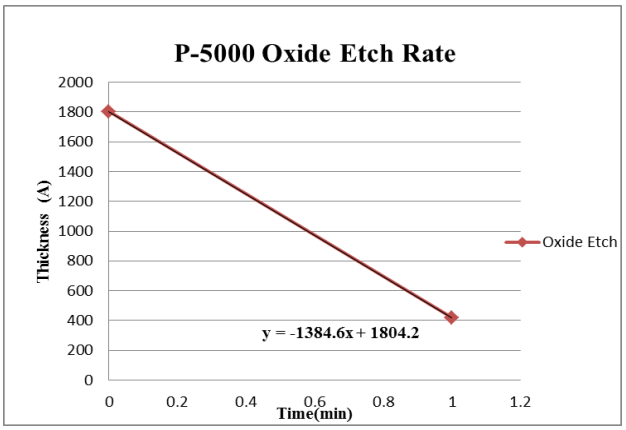

Figure 17. Thermal Oxide Etch Rate in the P-5000 Chamber C RIE.

The etch rate above is used to etch the 400nm oxide layer utilizing the aluminum hard mask to allow the creation of the oxide mandrel.
The following figures are the results of the RIE of the thermal oxide:

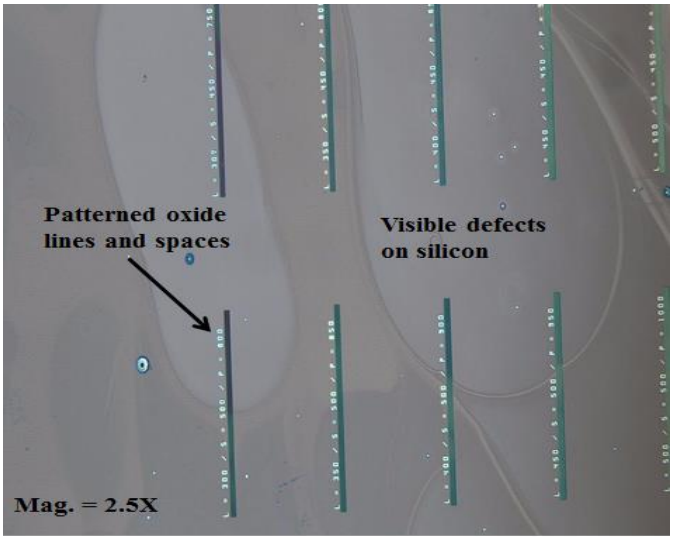

Figure 18. OM Image of the RIE Oxide Patterning Utilizing Sputtered Aluminum Mask.

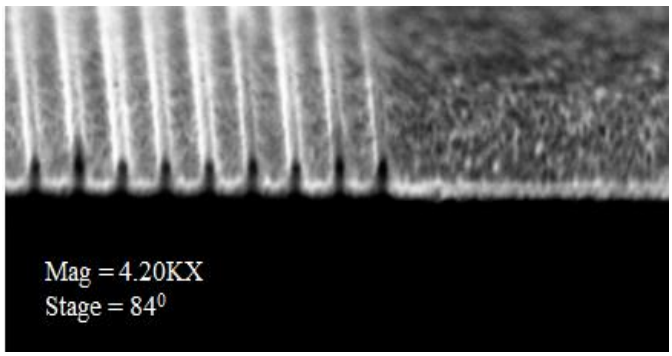

Figure 19. SEM Image of the RIE Oxide Pattrening with the Sputtered Aluminum Mask.

As seen in figure 18, the RIE of oxide left visible defects on the silicon surface, even when running the sample in an RIE for longer time. SEM is used to investigate the sample. Figure 19 shows an SEM image that appears to have a spiking effect. This effect is the result of the remaining silicon from the sputtered aluminum; the sputtered aluminum source is composed of 99% aluminum and 1% silicon. The aluminum RIE did not remove the silicon from the surface of the oxide, and it carried on through the oxide etch which resulted in non-uniform etching with spiking effect.

This problem is solved by evaporating a 100% pure aluminum element onto the oxide surface followed by a lithography and an RIE step to define the desired features on aluminum following the exact same steps.

The following figures (20, 21, and 22) show successful oxide RIE patterning with the evaporated aluminum mask.

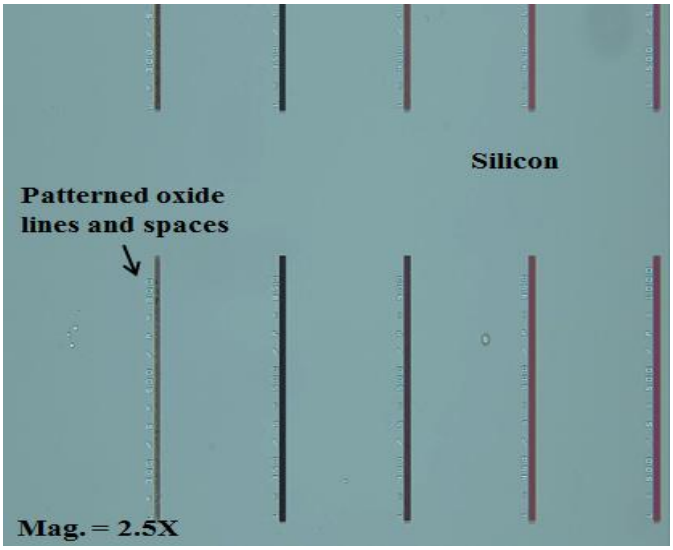

Figure 20. OM Image of the RIE Oxide Patterning Utilizing Evaporated Aluminum Mask.

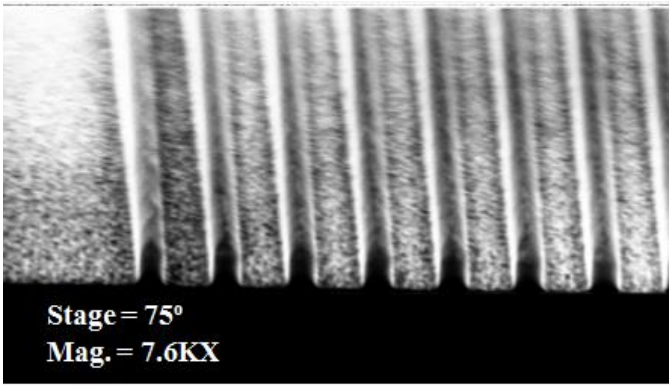

Figure 21. SEM Image of the RIE Oxide Patterning Utilizing the Evaporated Aluminum Mask.

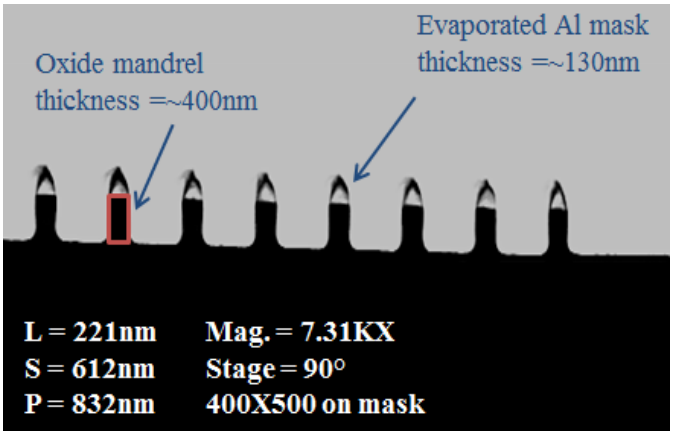

Figure 22. SEM Cross Section Image of the RIE Oxide Patterning Utilizing the Evaporated Aluminum Mask.

The evaporated aluminum mask solved the previous problem since it does not contain any other element with aluminum. This successful pattern transfer resulted in 221nm lines and 612nm spaces on a 832nm pitch.

The nitride deposition step was done via LPCVD which allowed the formation of the nitride on the oxide mandrel. The CD of the sidewall spacers can be controlled by altering the nitride thickness; a layer of 200nm would result in a line width of 200nm.

Figures 23 and 24 depict the 200nm conformal nitride deposition after removing the aluminum mask.

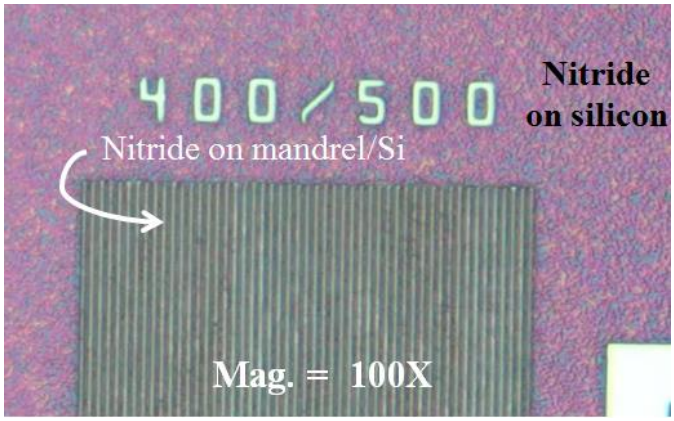

Figure 23. OM Image of the LPCVD Nitride Layer on the Oxide Mandrel.

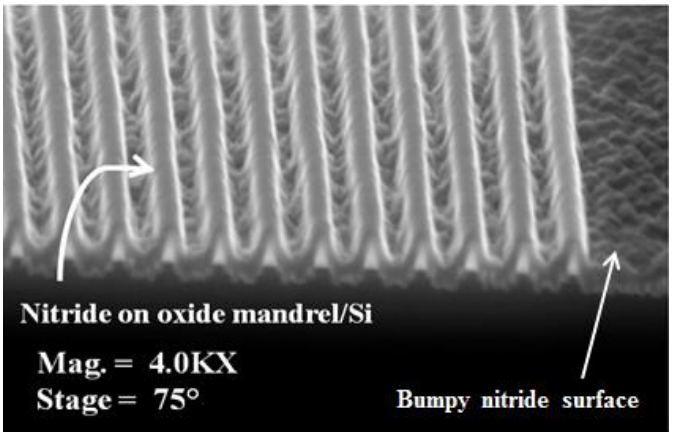

Figure 24. SEM Image of the LPCVD Nitride Layer on the Oxide Mandrel.

The nitride thickness was measured on a monitor wafer with 380nm of oxide and was found to be approximately 180nm. The nitride deposition is conformal around the oxide mandrel as expected, but with a textured surface. The nitride surface topography can be due to the remaining oxide that is not completely etched off in RIE, or the silicon surface is over etched during the oxide etch; these two cases can result in some surface topography that can be transferred to the nitride film.
The third case could be that the gas flow during the nitride deposition is too fast. This textured effect can directly affect the subsequent nitride etch when forming the sidewall spacers.

Figure 25 shows the etch rate of the LPCVD nitride that was done on a un-patterned wafer utilizing the Drytek RIE tool.

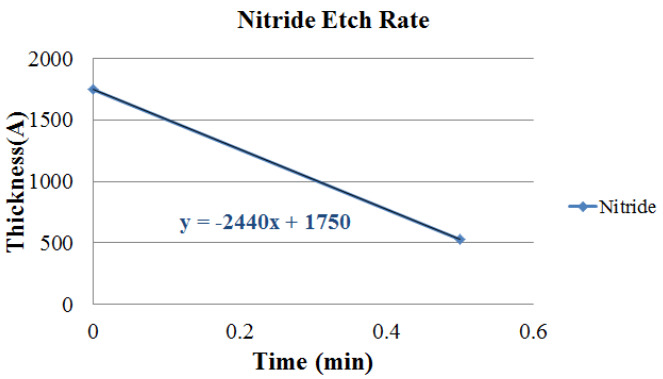

Figure 25. Nitride Etch Rate in the Drytek Chamber 2 RIE.

The etch rate was measured to be 244nm/min. In most cases, the etch rate on a flat surface is different compared to the etch rate on a patterned surface. Thus, a time etch was performed to accurately etch the nitride in the space between the oxide mandrels so to form the nitride sidewall spacers.

Figure 26 and 27 shows the nitride timed etch that was performed in the Drytek at 30 and 40 seconds.

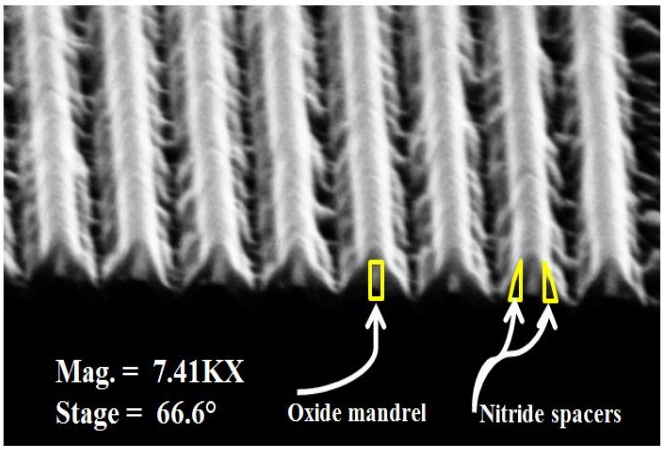

Figure 26: SEM Image of the RIE Nitrde for 30 Seconds.

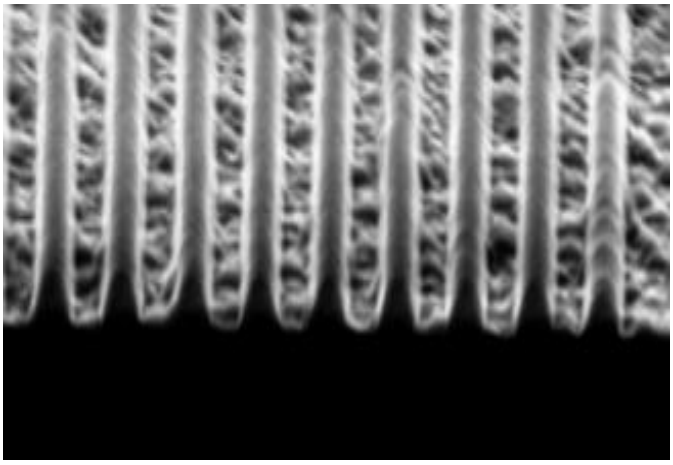

Figure 27: SEM Image of the RIE Nitrde for 40 Seconds.

It was clearly observed that the texture effect in the nitride film caused a non-uniform spacer etch. As seen in figure 26, the topographic surface of the nitride film caused a non-uniform etch in between the oxide mandrel which directly affected the side wall spacer profile. This sidewall spacer mask will be useless if utilized for the subsequent silicon etch and it will defeat the purpose of having dense, equal line and space features. Figure 27 shows the over etch of the nitride spacers and the undesired initial silicon etch.

The main key to solve the nitride etch problem is by achieving a uniform conformal nitride deposition since it proved that it can directly affect the subsequent sidewall spacer etch to form 200nm features.

V. CONCLUSION

The resist features were successfully patterned through annual illumination setting with 280nm critical dimension. The evaporated pure aluminum mask is excellent for oxide etching, creating the oxide mandrel with an anisotropic profile. Over-etching the aluminum mask proved beneficial for achieving 211nm features.

The LPCVD nitride film shows a conformal yet textured profile over the oxide mandrel. The nitride surface topography resulted in non-uniform opening between nitride sidewall spacers which directly affected the nitride sidewall spacer profile.

To improve this experimental procedure, a design of experiment is needed to investigate the nitride deposition to minimize the surface topography effect as well as optimizing the nitride etch recipe for an optimal sidewall profile. Also, a hard mask under the nitride spacers is considered for the silicon etch.

APPENDIX

Process	Tool/Recipe
Oxied Growth (400nm)	Tool: Bruce urnace Tube 1. Recipe: 341 LFull wet 4000A Ox.
Aluminum Deposition	Tool: CHA Flash Evaporator.
I-CON ARC 7 Coating	Tool: SSI wafer track. HMDS: No Dehydration: 150C, 60 sec. Cool: 15 sec. Spin Speed: 800RPM. Soft Bake: 170, 60sec Cool: 15 sec.
Diluted OiR 620 Coating	Tool: SSI wafer track. HMDS: No Dehydration: No Cool: No Spin Speed: 1000RPM. Soft Bake: 95, 60sec Cool : 15 sec.
Exposure	Tool: ASML PAS 5500 i-line Stepper. Dose: 170mj/cm2 Focus: -0.4 NA = 0.6 $\sigma i = 0.535$ $\sigma o = 0.9$
OiR 620 Develop	Tool: SVG wafer track. PEB: 110, 60 sec. Cool: 15 sec.

	Develop: 45 sec. Hard Bake: 145, 60sec Cool: 15 sec.
I-CON ARC 7 Etch	Tool: Drytech Chamber 2. Recipe: O2 Ash Power: 200W. Pressure: 70mT O2: 5sccm.
Aluminum Etch	Tool: LAM4600 Recipe: 122122.
Oxide Etch	Tool: P-5000 Chamber C. Power : 500W. Pressure: 250mT. O2: 10 sccm. CHF3: 100 sccm. CHF4: 100 sccm.
Nitride Deposition	Tool: LPCVD Furnace Recipe: Nitride 810C. Base Pressure: 68mT. Dep. Pressure: 297mT. DCS: 160sccm. NH3: 190sccm. Time: 33min.
Nitride Etch	Tool: Drytek Chamber 2. Power: 250W. Pressure: 40mT. CHF3: 30 sccm. SF6: 30 sccm.

ACKNOWLEDGMENT

Salwan Omar thanks Dr. Pearson and Dr. Ewbank for their advisement and project support, Dr. Fuller for providing etching recipes, Dr. Rommel and Dr. Thomas for the SEM training and certification, and Dr. Kurinec for providing useful references. Additionally the support of the SMFL staff, including but not limited to: Patricia Meller and Sean O'Brien for their daily support and tool certification, Bruce Tolleson for his technical support on the LPCVD furnace, Rich Battaglia for his technical support on the CHA Flash evaporator, John Nash for his technical support on the CVC601, Peter Morici for his technical support on the Bruce furnace, and Tom Grimsley for writing the mask and for the lab access. Finally, a thank you to PROLITH by KLA-Tenor for providing the students with access to lithography simulation.

REFERENCE

[1] C. Shay, "CD Reduction through Annular Illumination and Sidewall Spacer Etch," ed. Rochester Institute of Technology, 2016.

[2] Development and Simulation of Sublithographic Process for nm Scale Features, 1st ed. Rochester: Wallace Memorial Library, 2010, pp. 57 – 84.

[3] E. Bowser, "Double Patterning Isolated and Dense Features With An ASML PAS 5500 i-Line Stepper," ed. Rochester Institute of Technology, 2013.

[4] M. Kucer, "Dry etching for High Aspect Ratio Silicon Fins," ed. Rochester Institute of Technology, 2014.

[5] S. Hadia, "FinFET Architechture Analysis and Fabrication Mechanism," vol. 8, Y. Kosta, Ed., ed. Charotar University of Science and Technology, 2011, pp. 235-240.

[6] X. Wei, H. L. Zhu, Y. B. Zhang, and C. Zhao, "Bulk FinFETs with body spacers for improving fin height variation," *Solid-State Electronics*, vol. 122, pp. 45-51, Aug 2016.